WHAT IS CLAIMED IS:

1. A magnetic memory, comprising:

a memory cell which has first and second resistive states;

first and second write conductors configured to conduct first and second currents to change the memory cell between the first and the second resistive states, wherein the first and the second write conductors are routed in first and second directions and intersect the memory cell;

first and second sense conductors configured to conduct a sense current through the memory cell; and

a sense circuit coupled to the second sense conductor configured to detect the change between the first and the second resistive states.

2. The magnetic memory of claim 1, wherein the sense circuit detects the change between the first and the second resistive states by detecting a change in the sense current through the memory cell which corresponds to the change between the first and the second resistive states.

3. The magnetic memory of claim 2, wherein the sense circuit comprises:

a voltage sense circuit configured to convert the sense current to a first input node voltage at a first input node;

an amplifier coupled between the first input node and a second input node configured to compare the first input node voltage to a second input node voltage at the second input node and provide an indication if the first input node voltage is not equal to the second input node voltage; and

an equalization circuit coupled between the first input node and the second input node configured to set the second input node voltage to be equal to the first input node voltage before the change between the first and the second resistive states is detected.

4. The magnetic memory of claim 3, wherein the equalization circuit includes a capacitor coupled to the second input node.

5. The magnetic memory of claim 4, wherein the equalization circuit includes a switch configured to have a closed position to set the second input node voltage to be equal to the first input node voltage before the change between the first and the second resistive states is detected, and wherein the amplifier detects the change between the first and the second resistive states when the switch is in an open position.

6. The magnetic memory of claim 3, wherein the voltage sense circuit is a voltage divider coupled between the first input node and a ground potential.

7. The magnetic memory of claim 3, wherein the first current is conducted through the first write conductor or the second current is conducted through the second write conductor until the amplifier provides the indication that the memory cell has changed between the first and the second resistive states.

8. The magnetic memory of claim 7, wherein the first current is set at a constant level and the second current is increased until the amplifier provides the indication that the memory cell has changed between the first and the second resistive states, and wherein the first current and the second current are reduced after the amplifier provides the indication.

9. The magnetic memory of claim 7, wherein the second current is set at a constant level and the first current is increased until the amplifier provides the indication that the memory cell has changed between the first and the second resistive states, and wherein the first current and the second current are reduced after the amplifier provides the indication.

10. The magnetic memory of claim 7, wherein the first current is increased and the second current is increased until the amplifier provides the indication that the memory cell has changed between the first and the second resistive

states, and wherein the first current and the second current are reduced after the amplifier provides the indication.

11. A magnetic memory sense system comprising:

a magnetic memory which includes a memory cell having first and second resistive states, wherein the magnetic memory includes first and second write conductors routed in first and second directions which intersect the memory cell, and wherein the magnetic memory includes first and second sense conductors configured to conduct a sense current through the memory cell; and

an amplifier circuit coupled to the second sense conductor and configured to detect a change between the first and the second resistive states of the memory cell by detecting a change in the sense current conducted by the first and the second sense conductor through the memory cell when the first and the second write conductor are conducting a first and a second current.

12. The sense system of claim 11, comprising a control system configured to change the memory cell between the first and the second resistive states by supplying a constant first current and increasing the second current until the memory cell changes between the first and the second resistive states, wherein the control system reduces the first and the second current after the memory cell has changed between the first and the second resistive states.

13. The sense system of claim 11, comprising a control system configured to change the memory cell between the first and the second resistive states by supplying a constant second current and increasing the first current until the memory cell changes between the first and the second resistive states, wherein the control system reduces the first and the second current after the memory cell has changed between the first and the second resistive states.

14. The sense system of claim 11, comprising a control system configured to change the memory cell between the first and the second resistive states by increasing the first and the second current until the memory cell changes

between the first and the second resistive states, wherein the sense system reduces the first and the second current after the memory cell has changed between the first and the second resistive states.

15. A magnetic memory, comprising:

a memory cell which has parallel and anti-parallel magnetic states;

first and second write conductors configured to conduct first and second currents to change the memory cell between the parallel and the anti-parallel magnetic states, wherein the first and the second write conductors are routed in first and second directions and intersect the memory cell;

first and second sense conductors configured to conduct a sense current through the memory cell; and

a sense circuit coupled to the second sense conductor configured to detect a change between the parallel and the anti-parallel magnetic states.

16. The magnetic memory of claim 15, wherein the sense circuit detects the change between the parallel and the anti-parallel magnetic states by detecting a change in the sense current through the memory cell which corresponds to the change between the parallel and the anti-parallel magnetic states.

17. The magnetic memory of claim 16, wherein the amplifier comprises:

a voltage sense circuit configured to convert the sense current to a first input node voltage at a first input node;

an amplifier having the first input node and a second input node configured to compare the first input node voltage to a second input node voltage at the second input node and provide an indication if the first input node voltage is not equal to the second input node voltage; and

an equalization circuit coupled between the first input node and the second input node configured to set the second input node voltage to be equal to the first input node voltage before the change between the parallel and the anti-parallel magnetic states is detected.

18. The magnetic memory of claim 17, wherein the equalization circuit includes a capacitor coupled to the second input node.

19. The magnetic memory of claim 18, wherein the equalization circuit includes a switch configured to have a closed position to set the second input node voltage to be equal to the first input node voltage before the change between the parallel and the anti-parallel magnetic states is detected, and wherein the amplifier detects the change between the parallel and the anti-parallel magnetic states when the switch is in an open position.

20. The magnetic memory of claim 17, wherein the voltage sense circuit is a voltage divider coupled between the first input node and a ground potential.

21. The magnetic memory of claim 17, comprising a control system configured to set the first current at a constant level and increase the second current until the amplifier provides the indication that the memory cell has changed between the parallel and the anti-parallel magnetic states, wherein the control system reduces the first current and the second current after the amplifier provides the indication.

22. The magnetic memory of claim 17, comprising a control system configured to set the second current at a constant level and increase the first current until the amplifier provides the indication that the memory cell has changed between the parallel and the anti-parallel magnetic states, wherein the control system reduces the first current and the second current after the amplifier provides the indication.

23. The magnetic memory of claim 17, comprising a control system configured to increase the first current and the second current until the amplifier provides the indication that the memory cell has changed between the parallel and the anti-parallel magnetic states, wherein the control system reduces the first current and the second current after the amplifier provides the indication.

24. A magnetic memory, comprising:

a first and second memory cell each having first and second resistive states;

a word line conductor pair extending in a first direction which intersects the first and the second memory cell, wherein the word line conductor pair includes a word write line and a word sense line, and wherein the word write line is configured to conduct a word write line current;

a first and second bit line conductor pair extending in a second direction which intersect the first and the second memory cells, wherein the first bit line conductor pair and the second bit line conductor pair each include a bit write line and a bit sense line;

a first sense circuit coupled to the bit sense line of the first bit line conductor pair and configured to detect a change between the first and the second resistive states of the first memory cell when the word write line of the word line conductor pair is conducting the word write line current and the bit write line of the first bit line conductor pair is conducting a first bit write line current, wherein the first sense circuit detects a change in a first bit sense current conducted through the first memory cell which corresponds to the change between the first and the second resistive states of the first memory cell; and

a second sense circuit coupled to the bit sense line of the second bit line conductor pair and configured to detect a change between the first and the second resistive states of the second memory cell when the word write line of the word line conductor pair is conducting the word write line current and the bit write line of the second bit line conductor pair is conducting a second bit write line current, wherein the second sense circuit detects a change in the second bit sense current conducted through the second memory cell which corresponds to the change between the first and the second resistive states of the second memory cell.

25. The magnetic memory of claim 24, comprising a control system configured to set the word write line current at a constant level and increase the

first bit write line current until the first sense circuit detects the change between the first and the second resistive states of the first memory cell and increase the second bit write line current until the second sense circuit detects the change between the first and the second resistive states of the second memory cell, wherein the control system reduces the first bit write line current after the first sense circuit detects the change between the first and the second resistive states of the first memory cell and reduces the second bit write line current after the second sense circuit detects the change between the first and the second resistive states of the second memory cell, and wherein the control system reduces the word write line current after both the first and the second sense circuits have detected the change between the first and the second resistive states of the first and the second memory cells.

26. The magnetic memory of claim 24, comprising a control system configured to set the first bit write line current and the second bit write line current at a constant level and increase the word write line current until both of the first and the second sense circuits have detected the change between the first and the second resistive states of the first and the second memory cells, wherein the control system reduces the first bit write line current after the first sense circuit has detected the change between the first and the second resistive states of the first memory cell and reduces the second bit write line current after the second sense circuit has detected the change between the first and the second resistive states of the second memory cell.

27. The magnetic memory of claim 24, comprising a control system configured to increase the word write line current and increase the first bit write line current until the first sense circuit detects the change between the first and the second resistive states of the first memory cell and increase the second bit write line current until the second sense circuit detects the change between the first and the second resistive states of the second memory cell, wherein the control system reduces the first bit write line current after the first sense circuit detects the change between the first and the second resistive states of the first

memory cell and reduces the second bit write line current after the second sense circuit detects the change between the first and the second resistive states of the second memory cell, and wherein the control system reduces the word write line current after both of the first and the second sense circuits have detected the change between the first and the second resistive states of the first and the second memory cells.

28. A magnetic memory, comprising:

a memory cell which has first and second resistive states;

first and second write conductors configured to conduct first and second currents to change the memory cell between the first and the second resistive states, wherein the first and the second write conductors are routed in first and second directions and intersect the memory cell;

first and second sense conductors configured to conduct a sense current through the memory cell; and

sense means to detect the change between the first and the second resistive states.

29. The magnetic memory of claim 28, wherein the sense means detects the change between the first and the second resistive states by detecting a change in the sense current through the memory cell which corresponds to the change between the first and the second resistive states; and wherein the sense means includes:

converter means to convert the sense current to a first input node voltage;

compare means to compare the first input node voltage to a second input node voltage and provide an indication if the first input node voltage is not equal to the second input node voltage; and

equalization means coupled between the first input node and the second input node configured to set the second input node voltage to be equal to the first input node voltage before the change between the first and the second resistive states is detected.

30. A method of detecting a change between a first and a second resistive state of a memory cell in a magnetic memory storage device which includes first and second write conductors which intersect the memory cell, comprising:

conducting first and second currents through the first and the second write conductors; and

detecting a change between the first and the second resistive states by detecting a change in a sense current conducted through the memory cell, wherein the change corresponds to the change between the first and the second resistive states.

31. The method of claim 30, further comprising:

wherein detecting the change comprises:

converting the sense current to a first input node voltage;

comparing the first input node voltage to a second input node voltage; and

providing an indication if the first input node voltage is not equal to the second input node voltage,

wherein comparing the first input node voltage to the second input node voltage comprises setting the second input node voltage to be equal to the first input node voltage before the first input node voltage is compared to the second input node voltage; and

wherein conducting the first and the second currents through the first and the second write conductors comprises:

setting the first current at a constant level;

increasing the second current;

providing the indication when the memory cell has changed between the first and the second resistive states; and

reducing the first current and the second current after the indication is provided.